

FIG. 1A
PRIOR ART

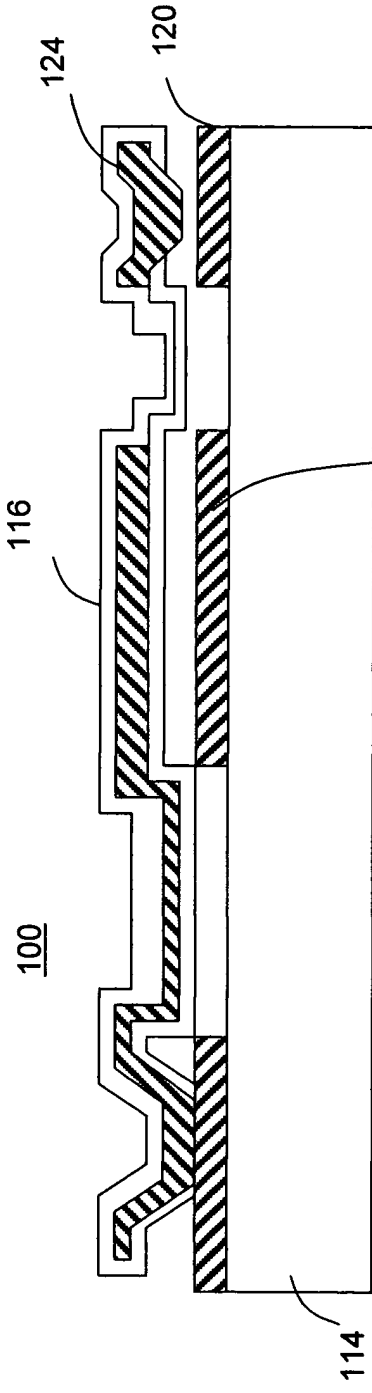


FIG. 1B
PRIOR ART

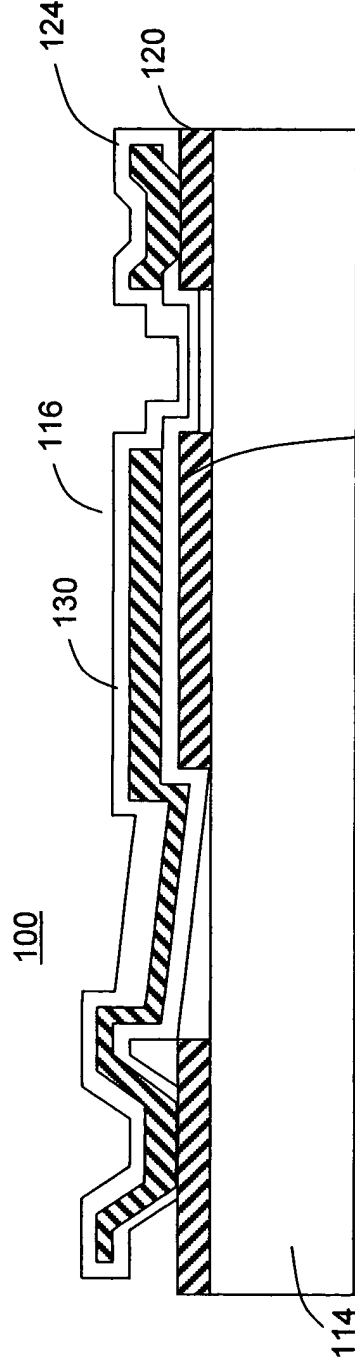


FIG. 1C
PRIOR ART

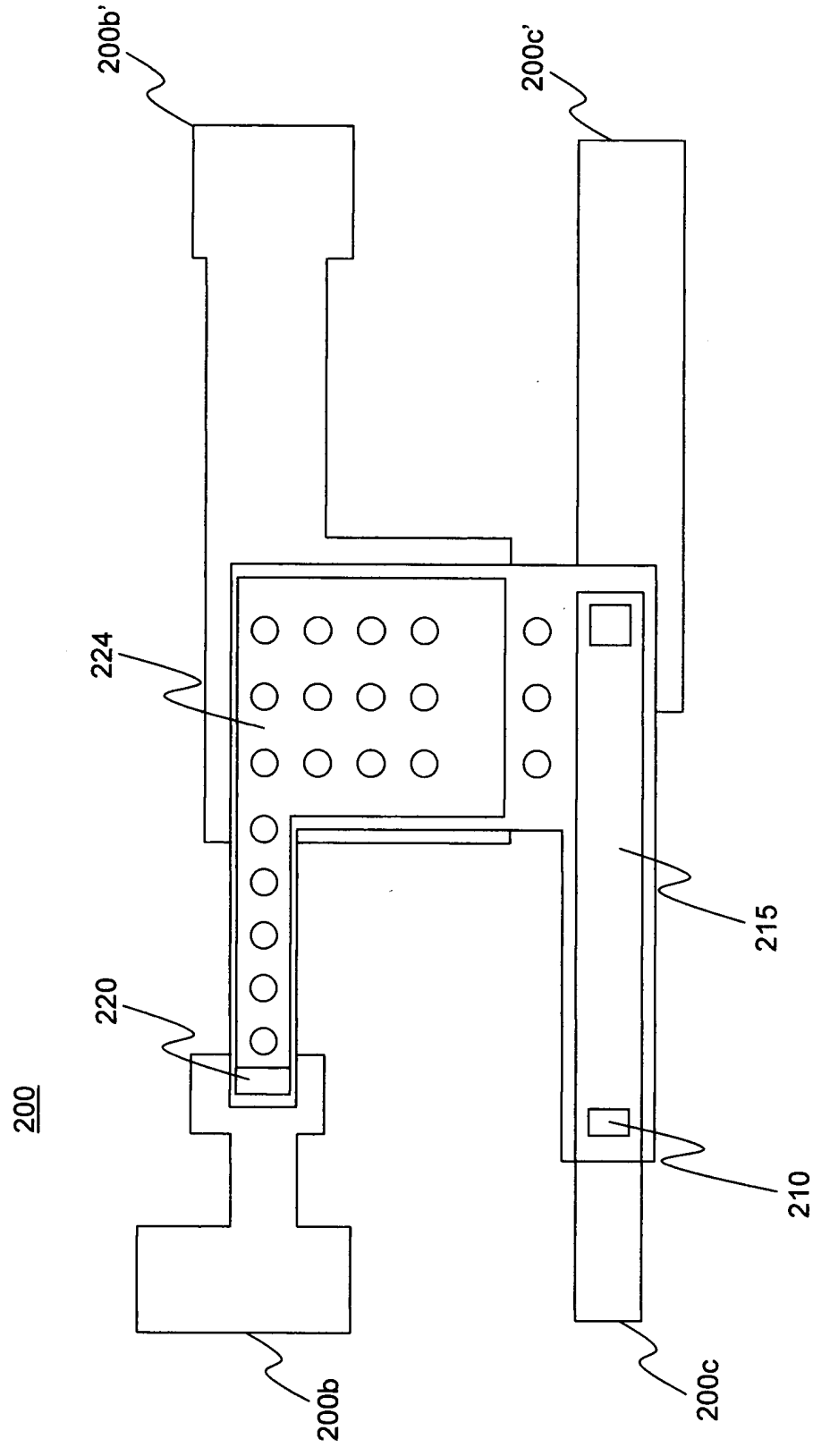


FIG. 2A
PRIOR ART

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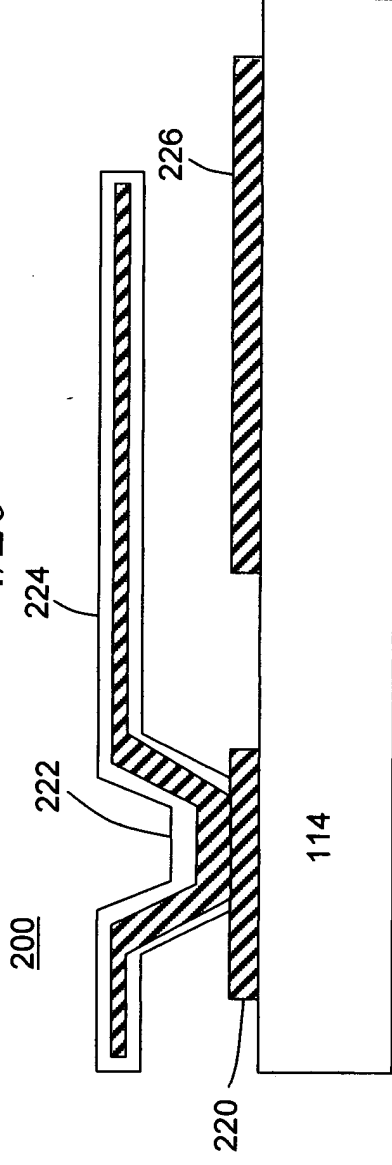


FIG. 2B
PRIOR ART

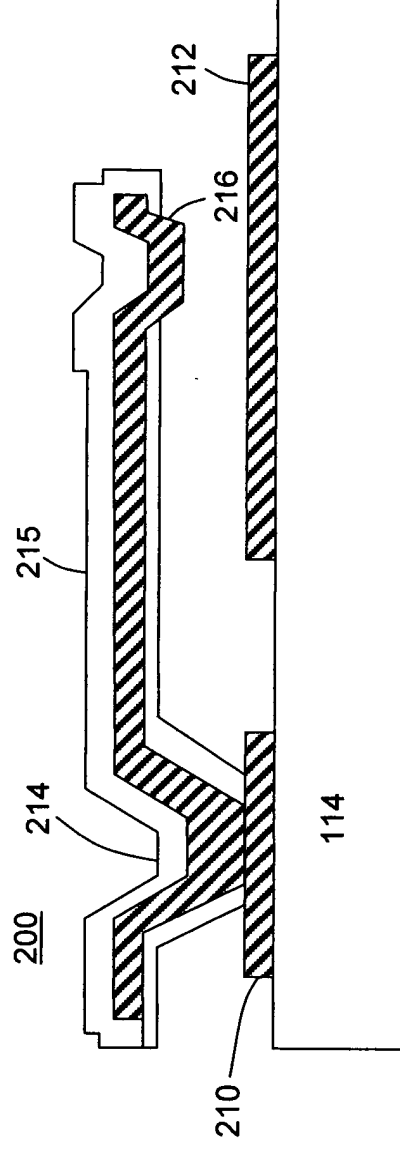


FIG. 2C
PRIOR ART

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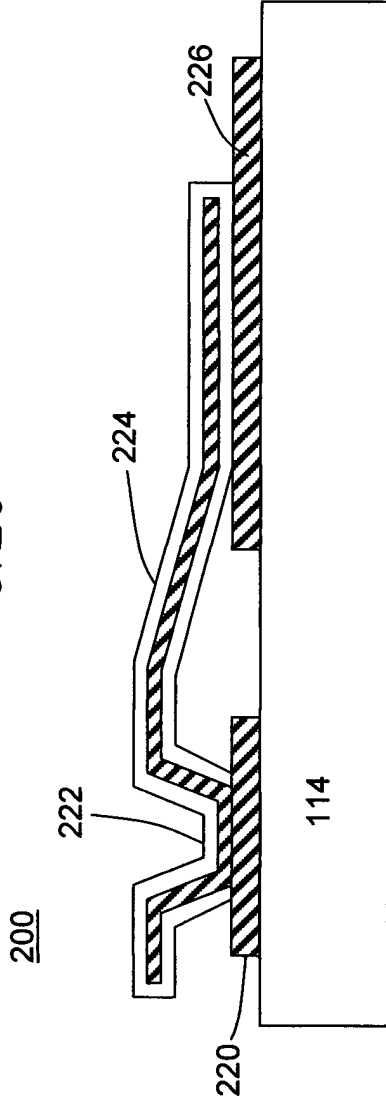


FIG. 2D
PRIOR ART

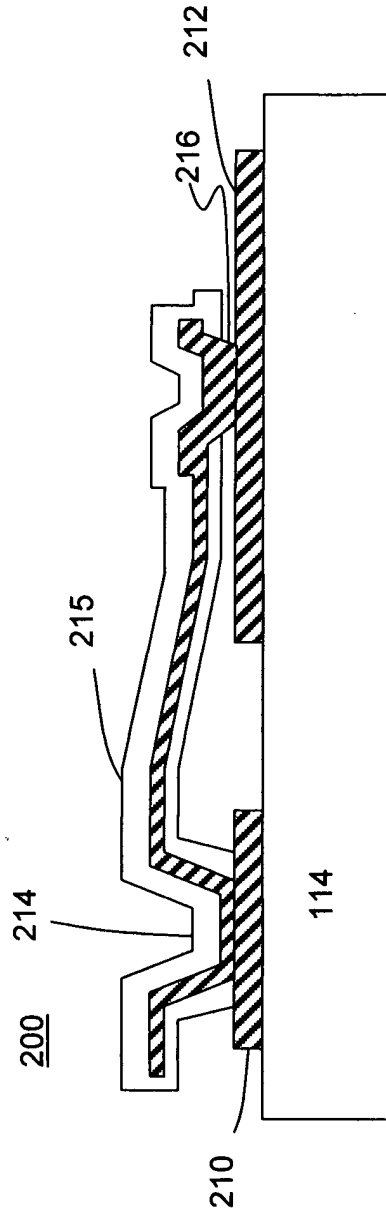


FIG. 2E
PRIOR ART

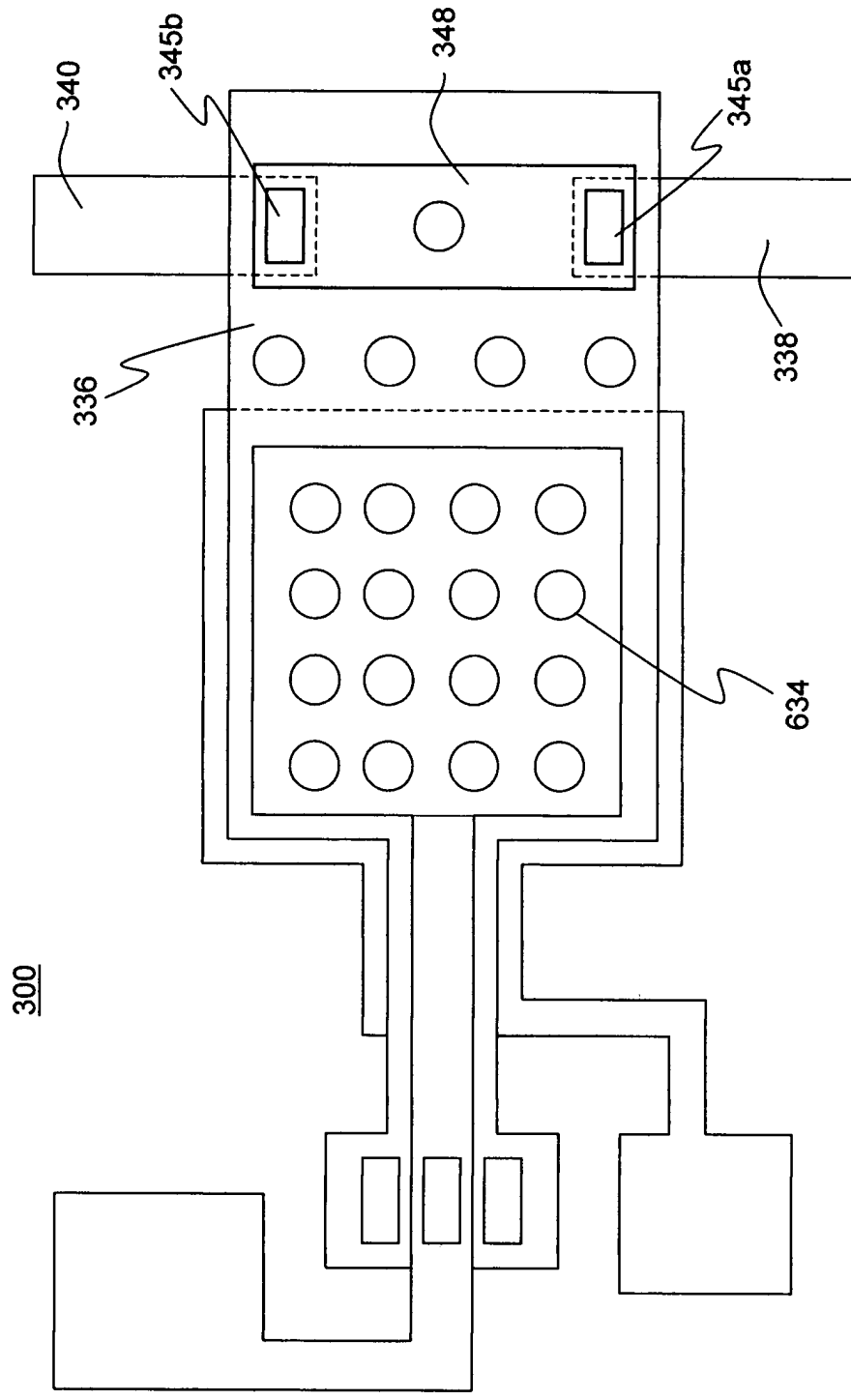


FIG. 3A

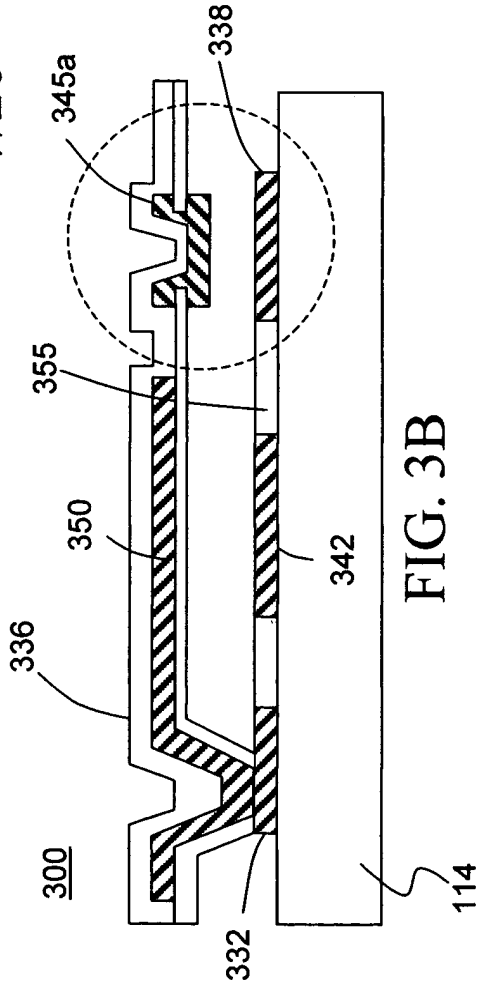
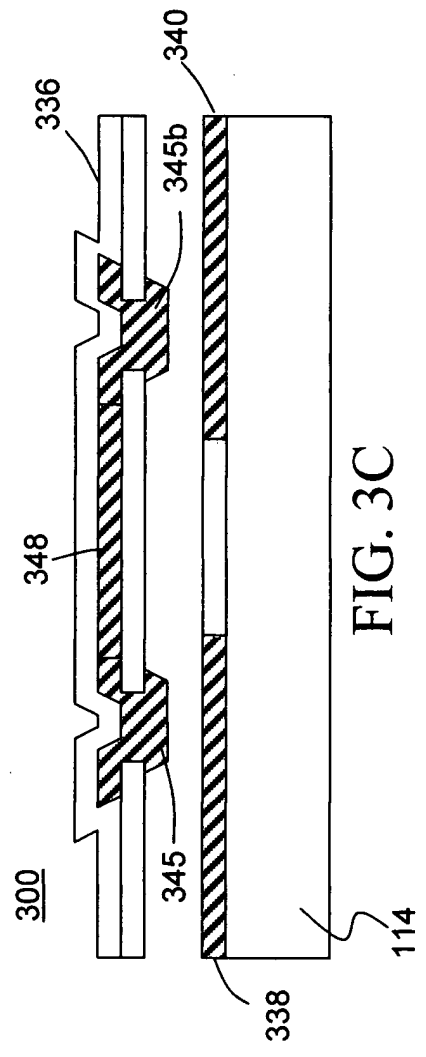
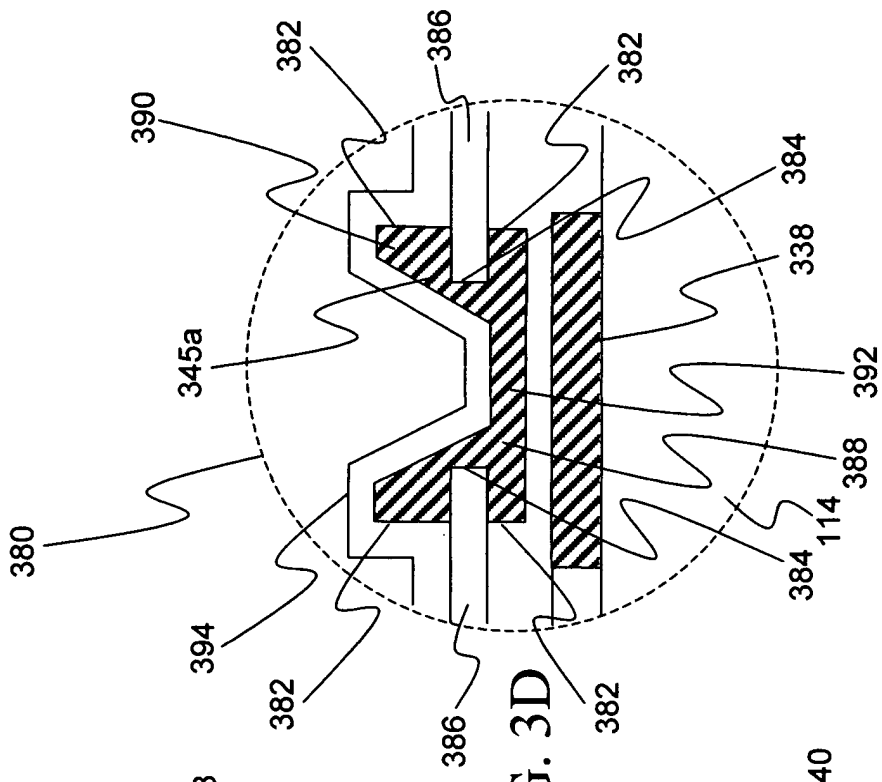
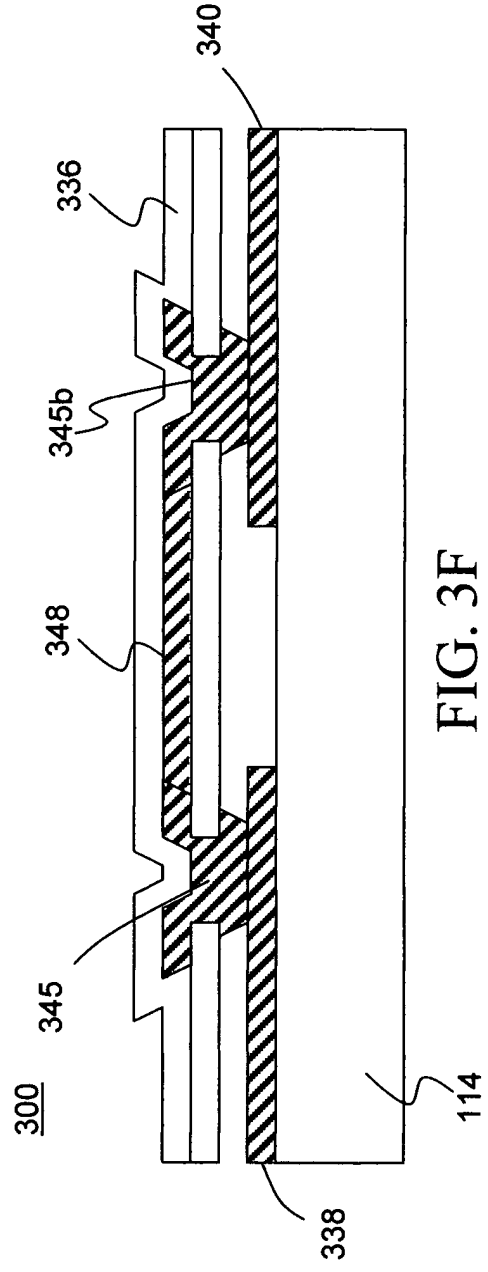
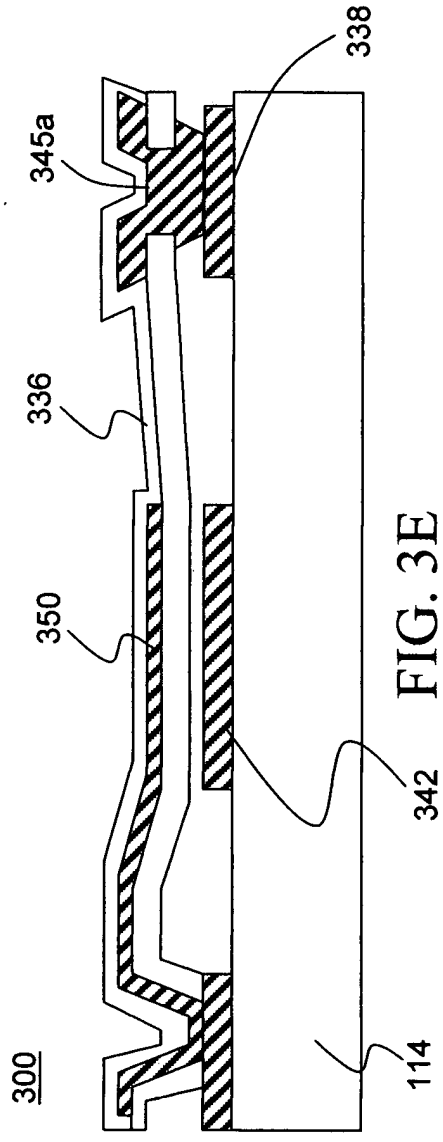


FIG. 3D





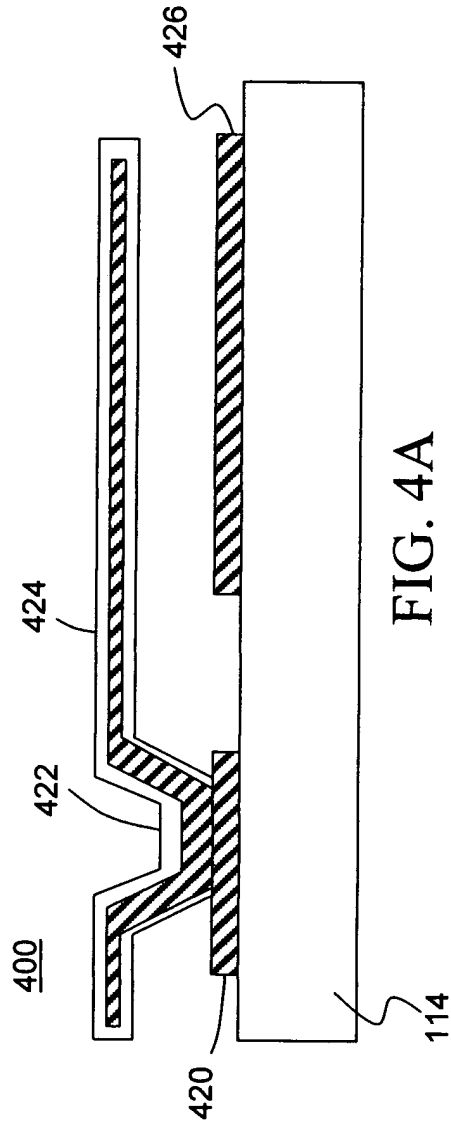


FIG. 4A

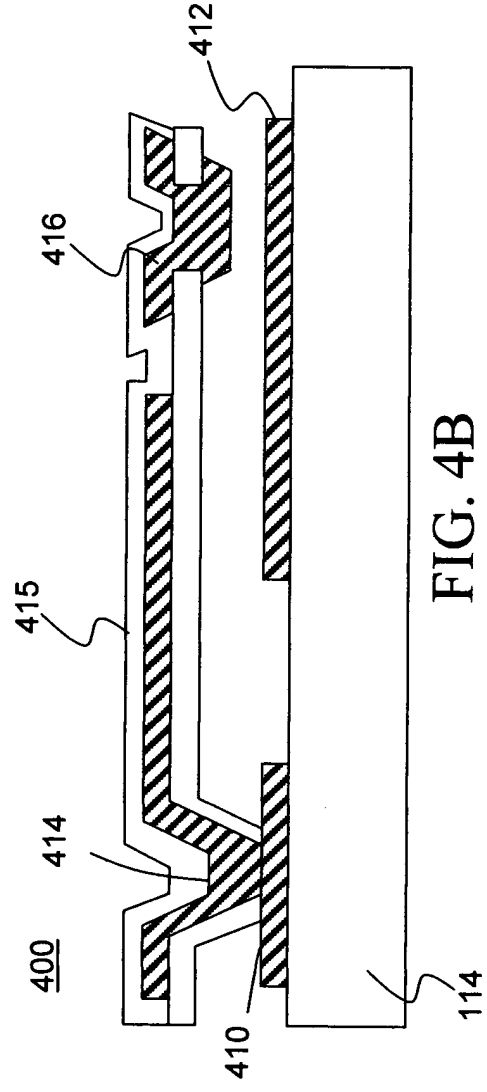


FIG. 4B

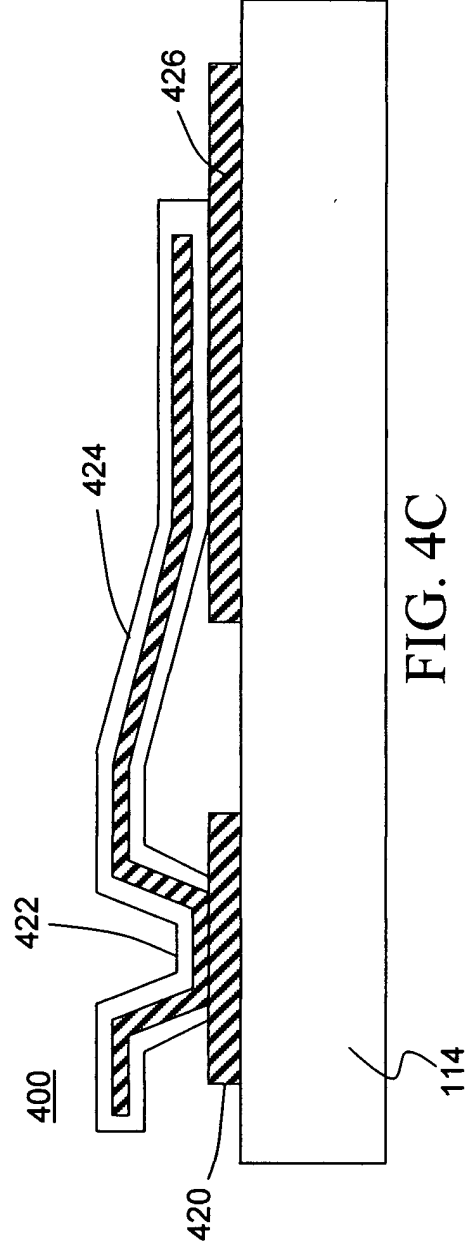


FIG. 4C

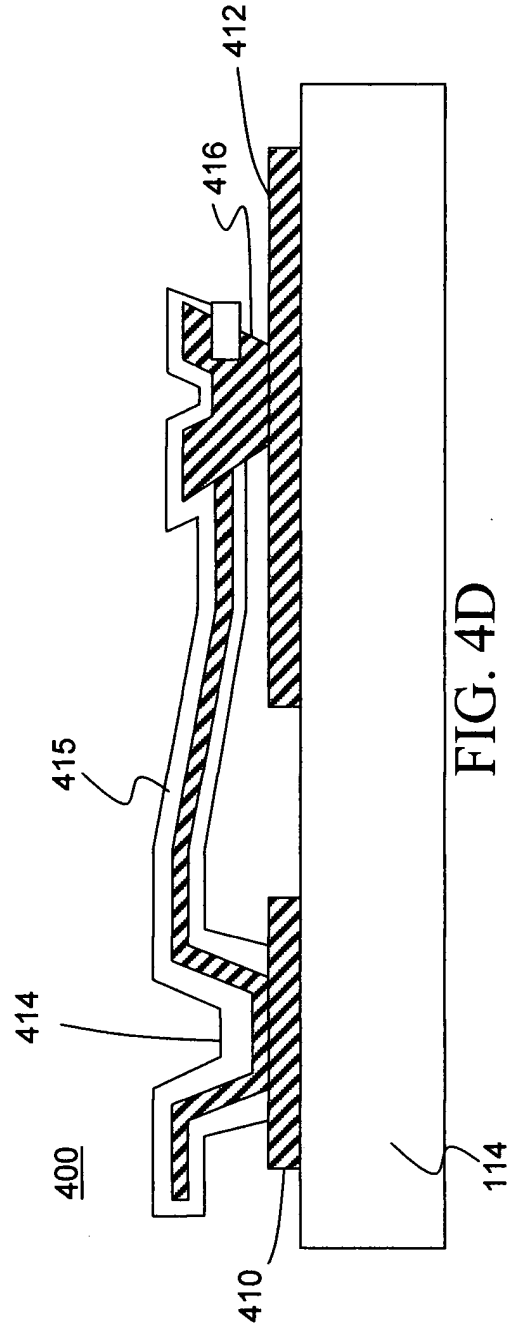


FIG. 4D

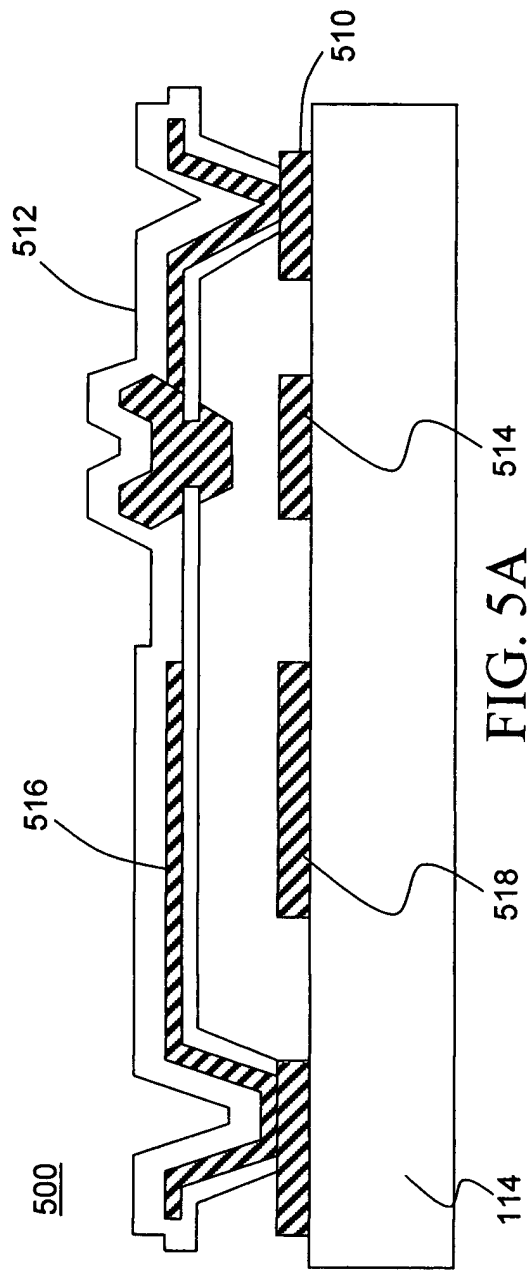


FIG. 5A

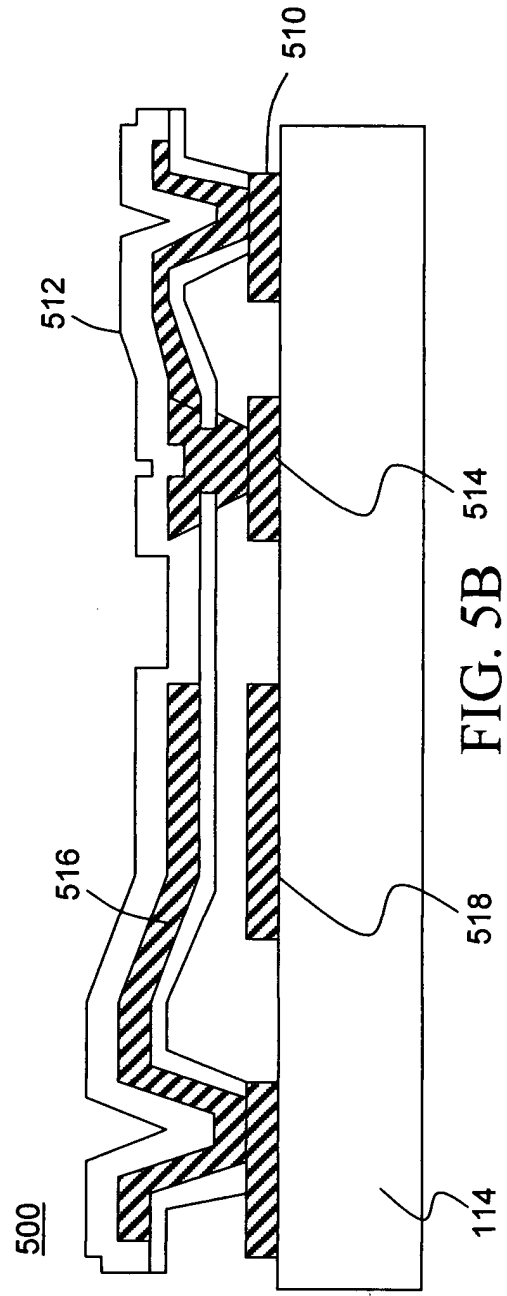
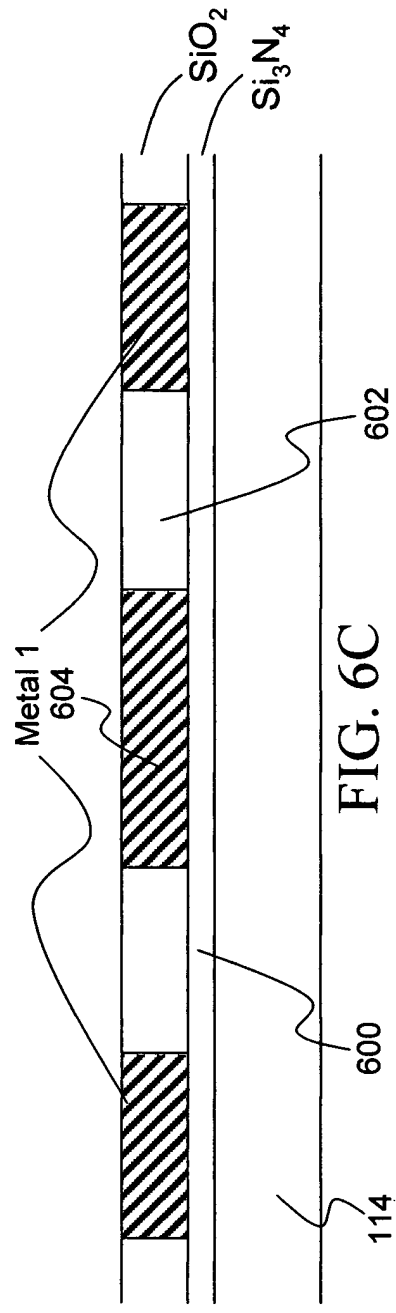
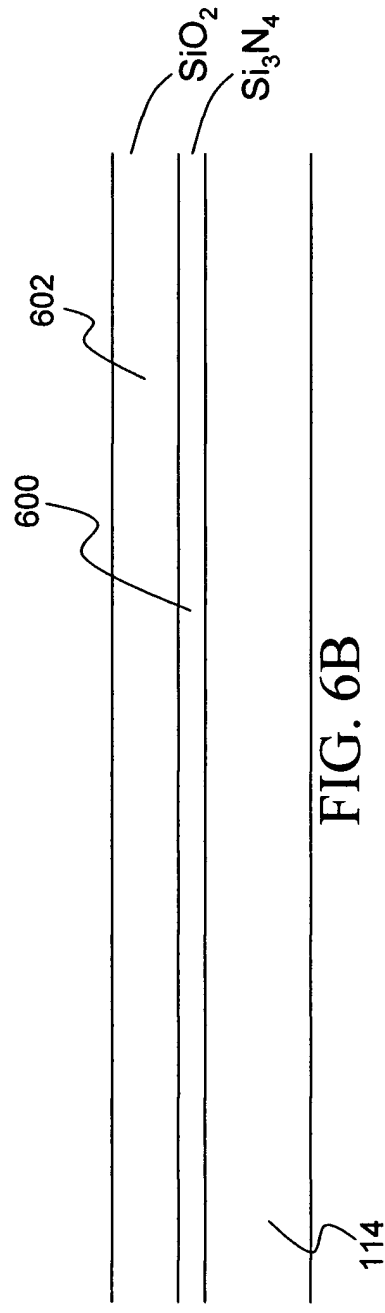
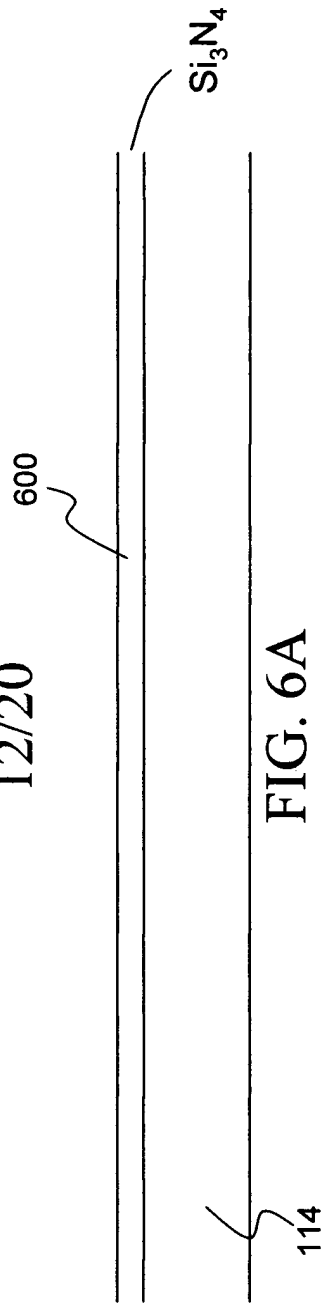


FIG. 5B



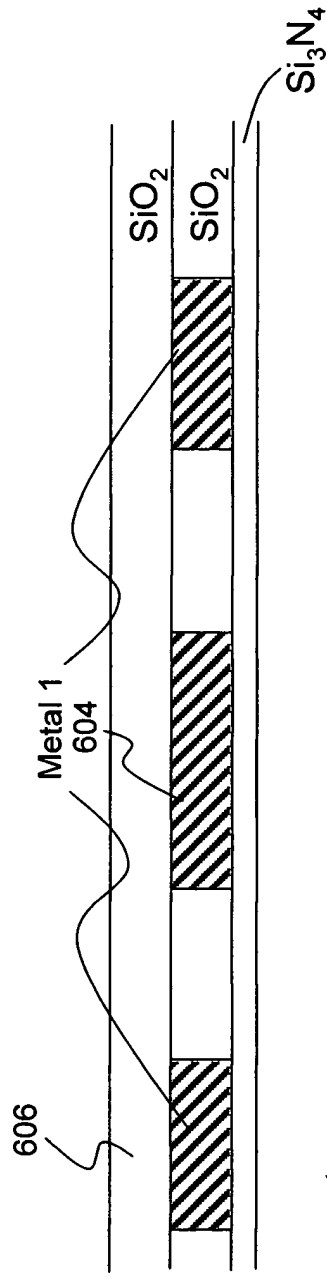


FIG. 6D

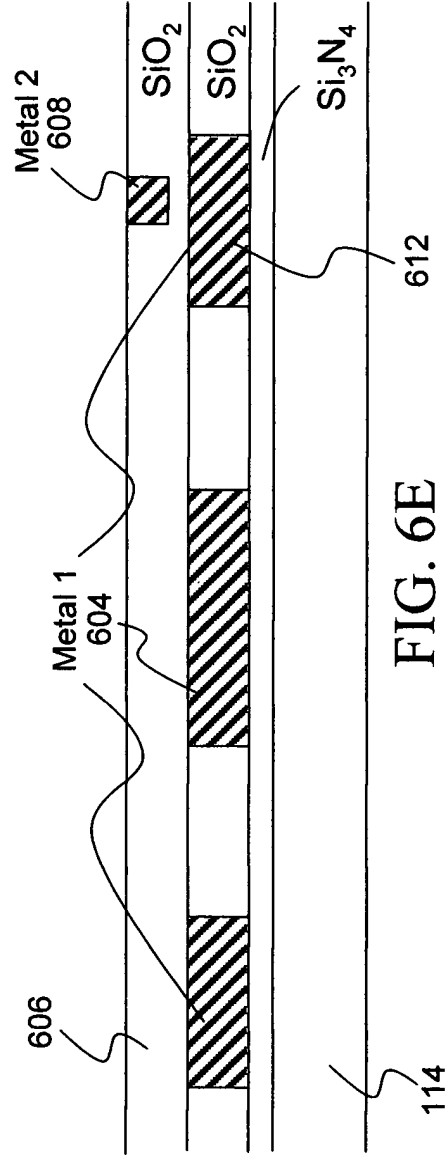
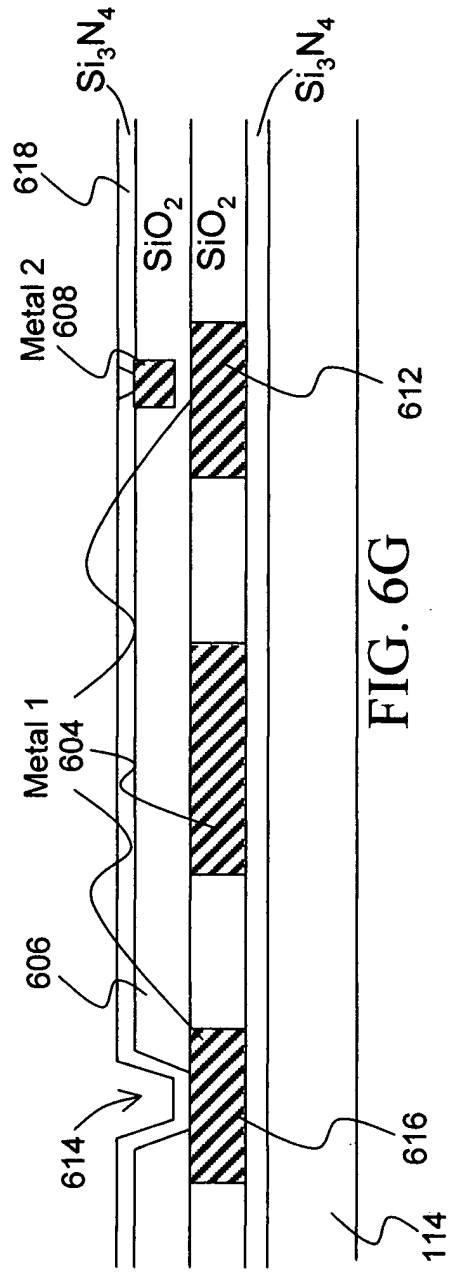
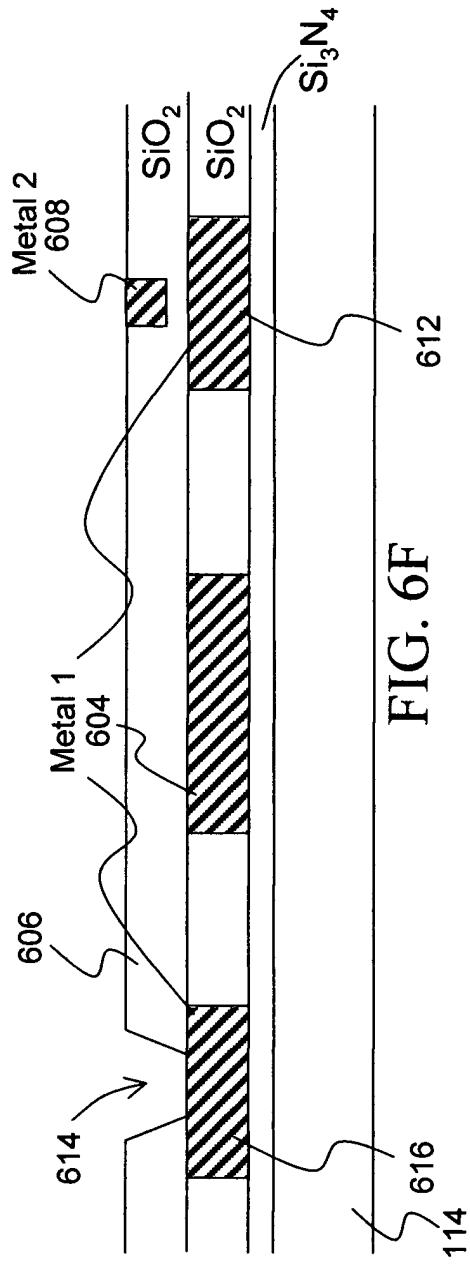
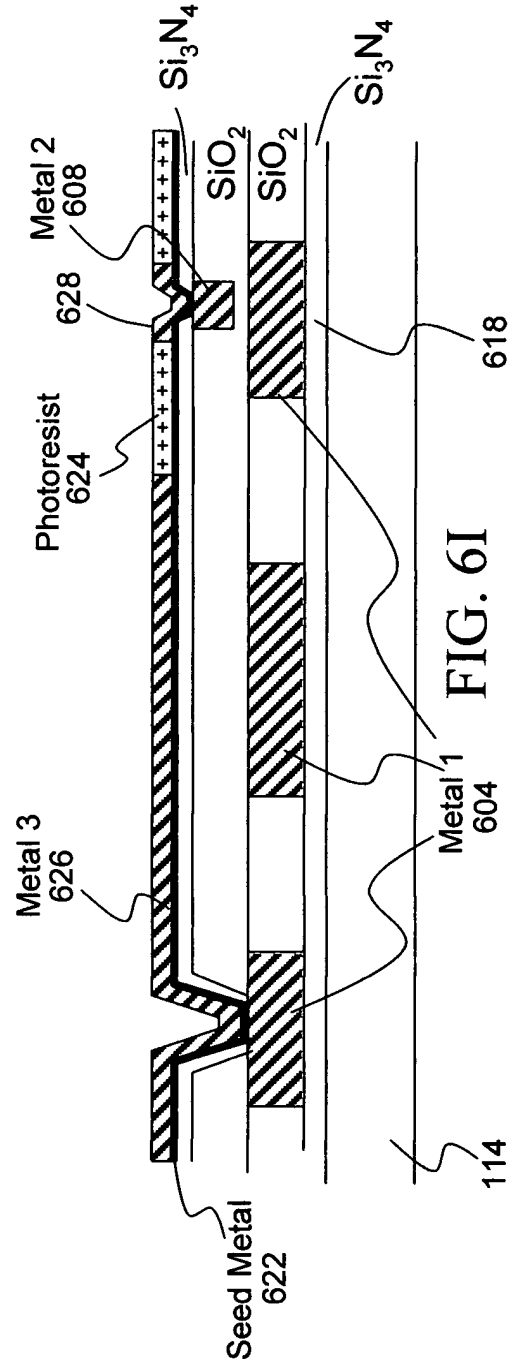
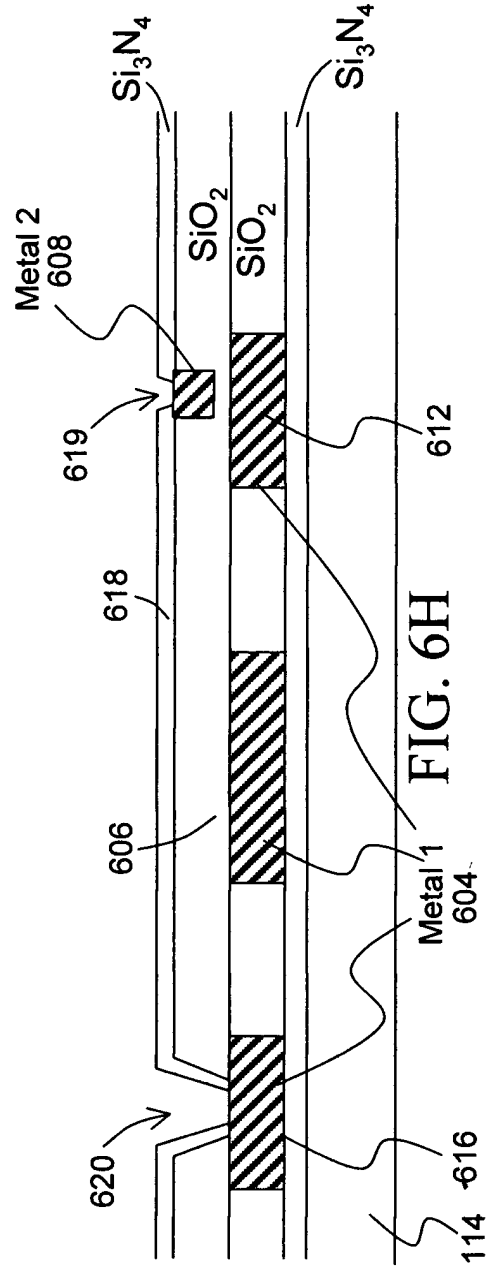


FIG. 6E





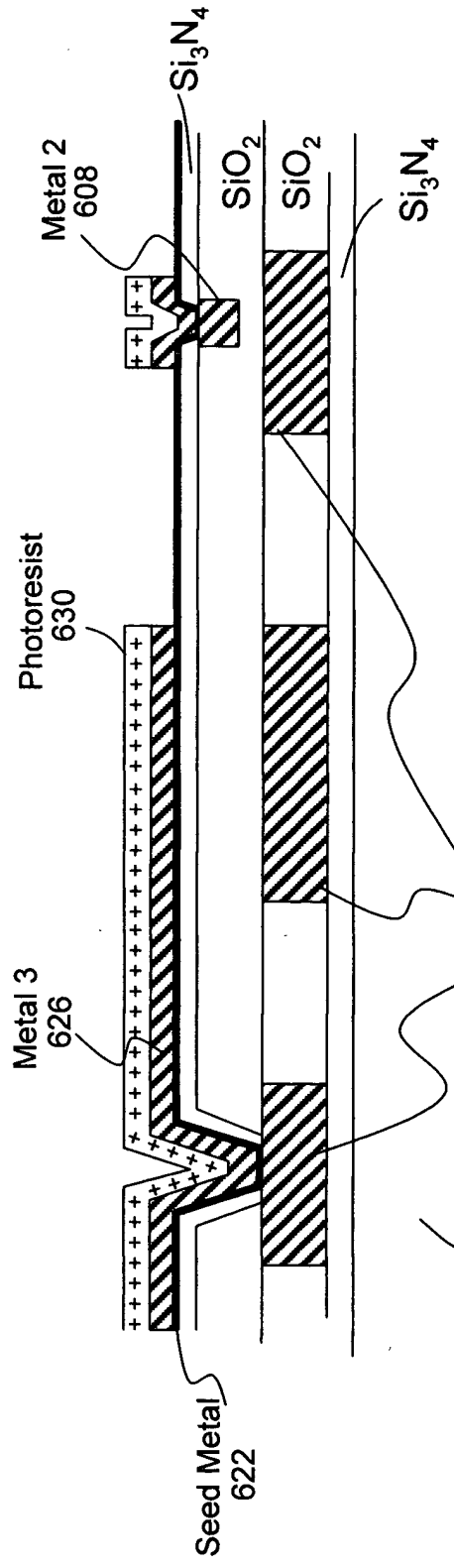


FIG. 6J

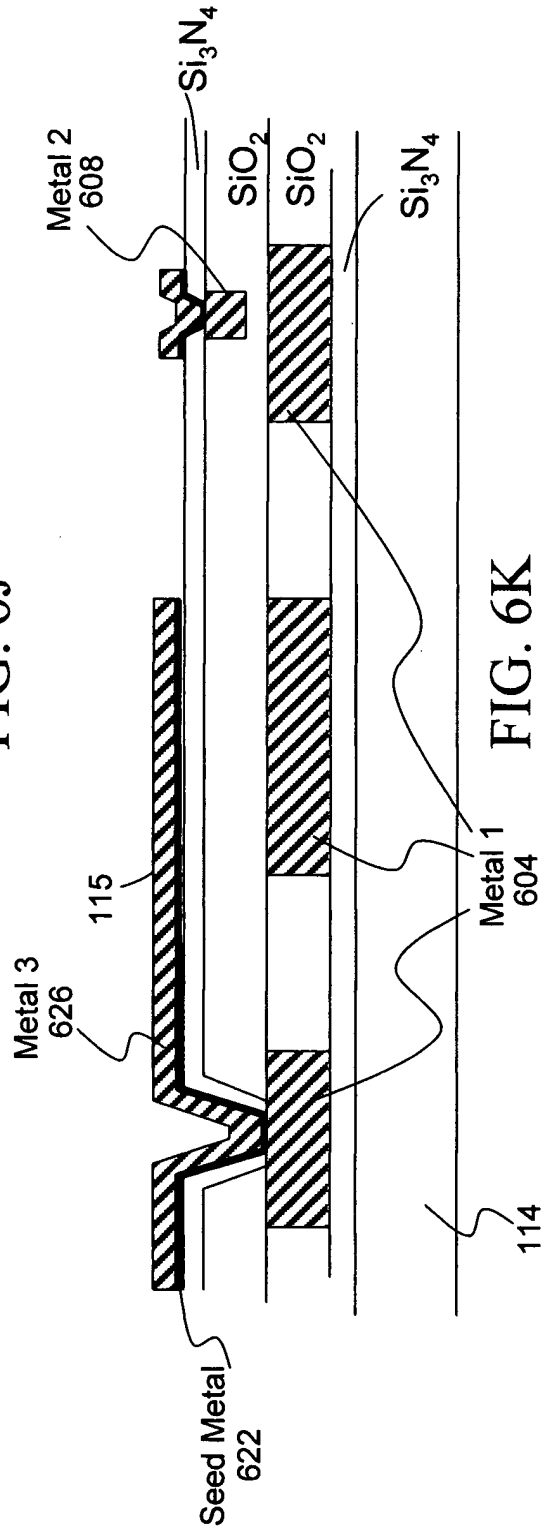


FIG. 6K

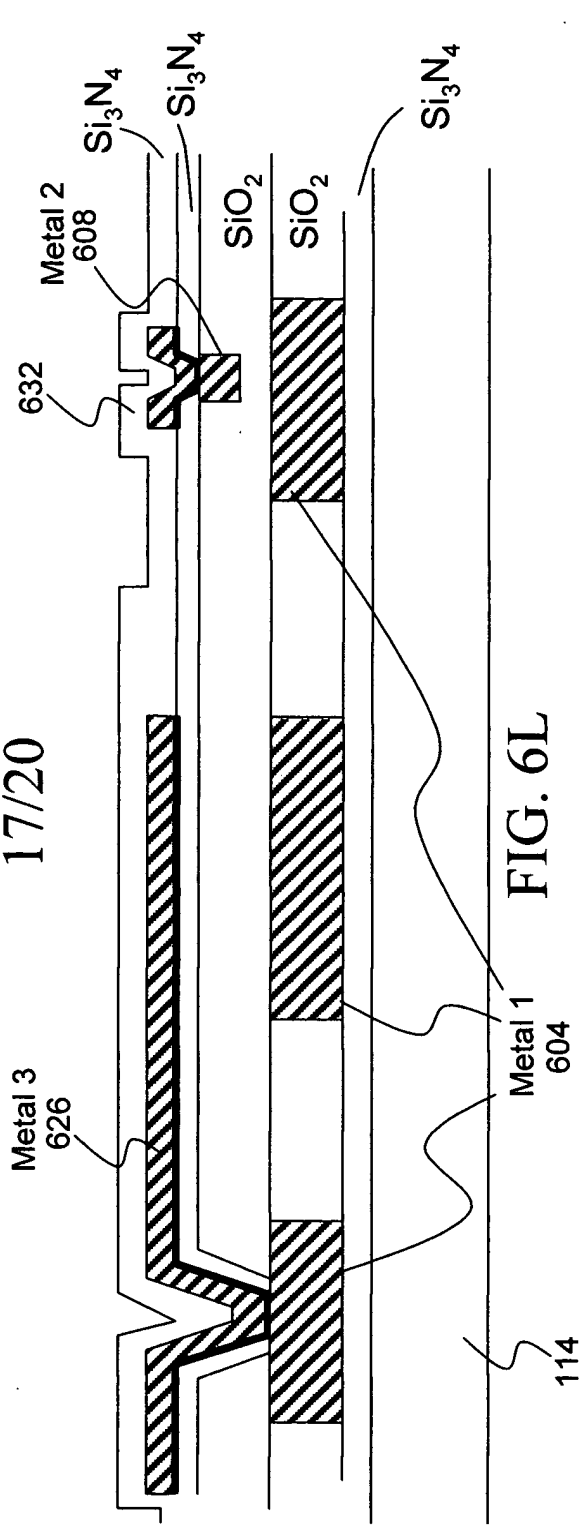


FIG. 6L

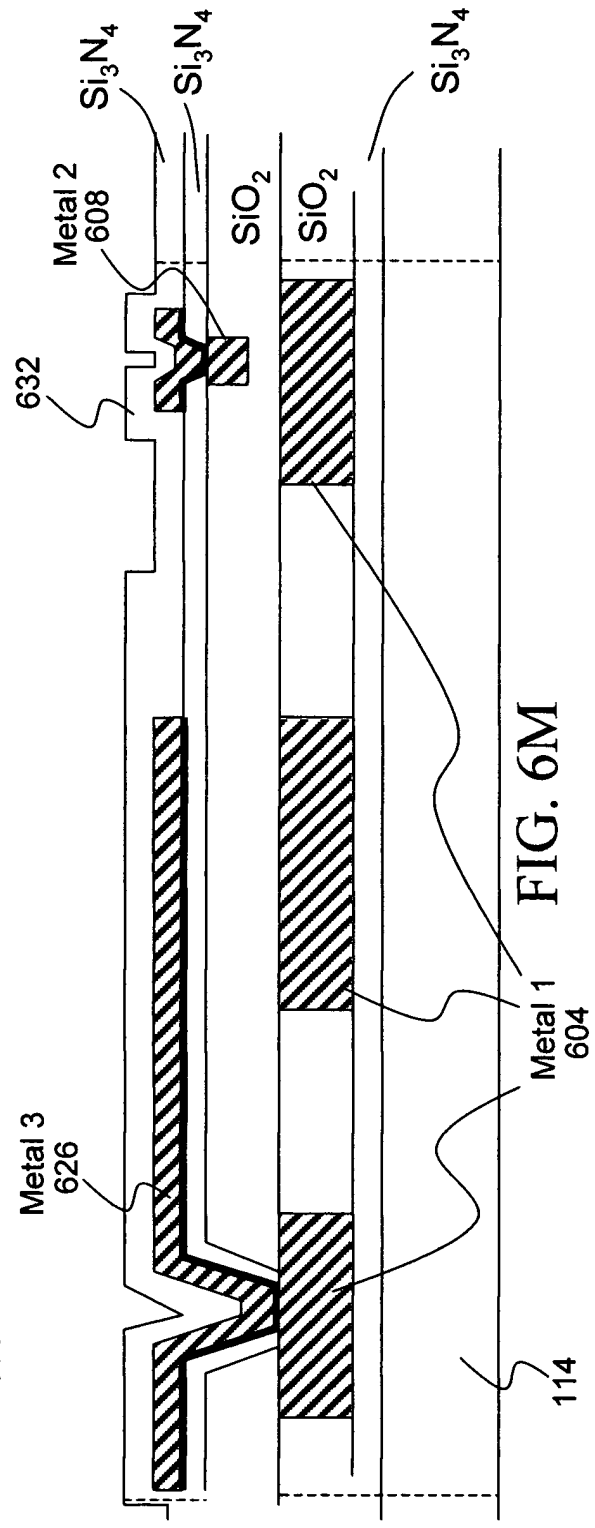


FIG. 6M

Layer	Materials	Deposit Process	Removal Process	Etch Process	Thickness
Substrate	Semiconducting Insulators, e.g., Silicon, GaAs, Quartz, Sapphire	N/A	N/A	N/A	300 μm - 600 μm
Dielectric Layer	Nitride, Oxide, Phosphorous Doped Oxide	PECVD, LPCVD	N/A	Wet Etch/Dry Etch	.1 μm - 5 μm
Photoresist	Positive Photoresist/Negative Photoresist	Spin Coat	Resist Stripper/Plasma Stripping	Spray Develop/Tank Develop	1 μm -8 μm
Substrate Electrodes	Gold/Any Conductor	E-beam Evaporation, Thermal Evaporation, Sputtering	N/A	Lift-off, Pattern and Etch	.5 μm -5 μm
Sacrificial Layer	Oxide, Silicon Metal (i.e., Al)	PECVD, LPCVD, E-Beam Evaporation	Wet Etch/Dry Etch	N/A	.5 μm -5 μm
1 st Insulating Layer	Nitride/Oxide	PECVD	N/A	Dry Etch	.5 μm -5 μm
Top Electrode Layer(s)	Gold/Any Conductor	E-Beam Evaporation, Thermal Evaporation, Plating	N/A	Wet Etch	.5 μm -5 μm
2 nd Insulating Structure Layer	Nitride, Oxide	PECVD	N/A	Dry Etch, Ion Milling	.5 μm -5 μm

FIG. 7

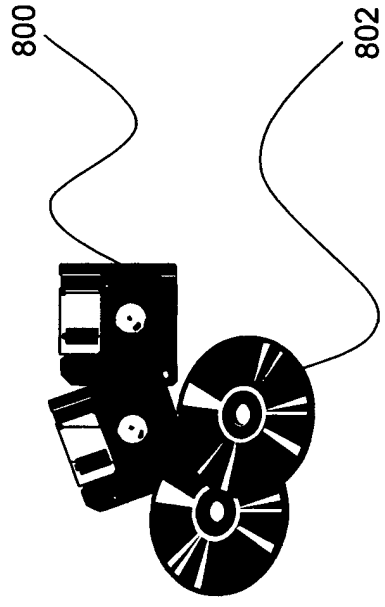


FIG. 8

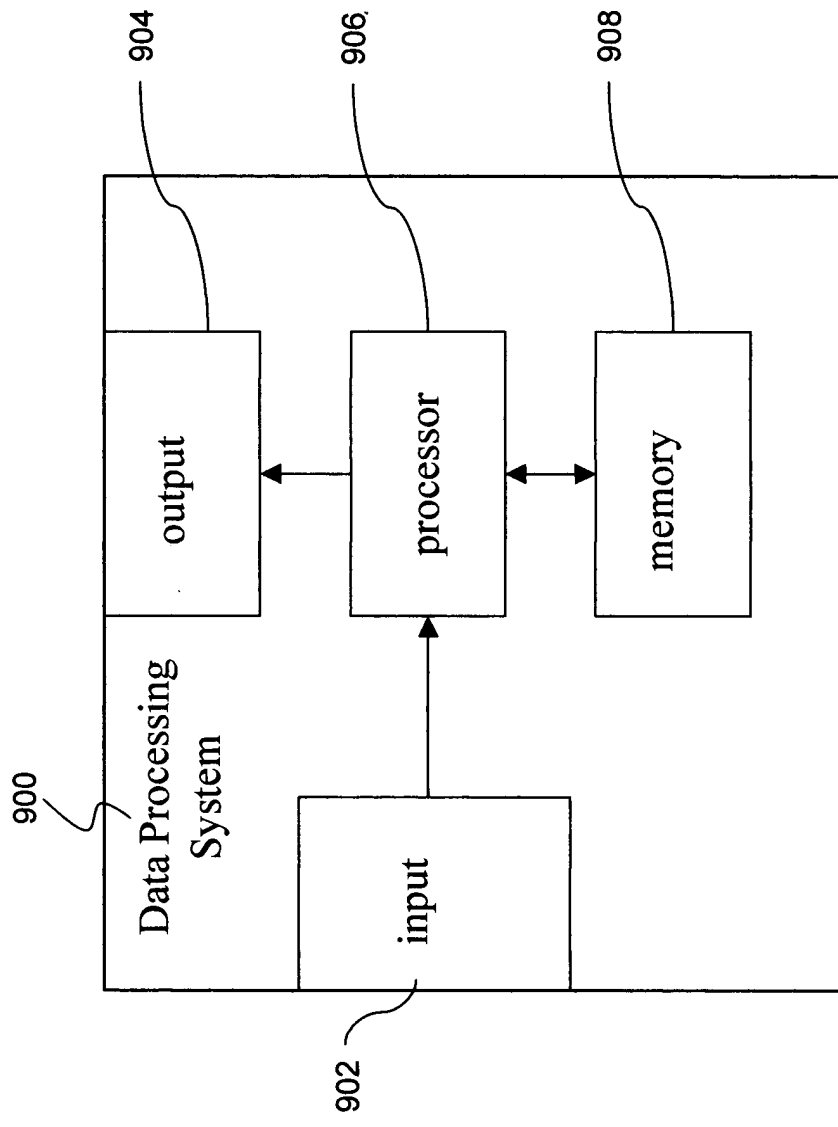


FIG. 9